TEXAS INSTRUMENTS

THS6002 Dual Differential Line Driver and Receiver Evaluation Module

User's Guide

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Mixed-Signal Products

SLOU018

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Preface

Related Documentation From Texas Instruments

- ***THS6002 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS*** (literature number SLOS202) This is the data sheet for the THS6002 amplifier integrated circuit used on the EVM.
- ***THS4001 HIGH-SPEED LOW-POWER OPERATIONAL AMPLIFIER*** (literature number SLOS206) This is the data sheet for the THS4001 amplifier integrated circuits used on the EVM.
- ***PowerPAD™ Thermally Enhanced Package*** (literature number SLMA002) This is the technical brief for the special PowerPAD package in which the THS6002 amplifier IC is supplied.

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Chapter 1

General Information

This chapter details the Texas Instruments (TI™) THS6002 Dual Differential Line Driver and Receiver Evaluation Module (EVM), SLOP117. It includes a list of EVM features, a brief description of the module illustrated with a pictorial and schematic diagrams, EVM specifications, details on configuring, connecting, and using the EVM, and a discussion on high-speed amplifier and PowerPAD package design considerations.

Topic **Page**

1.1 Features

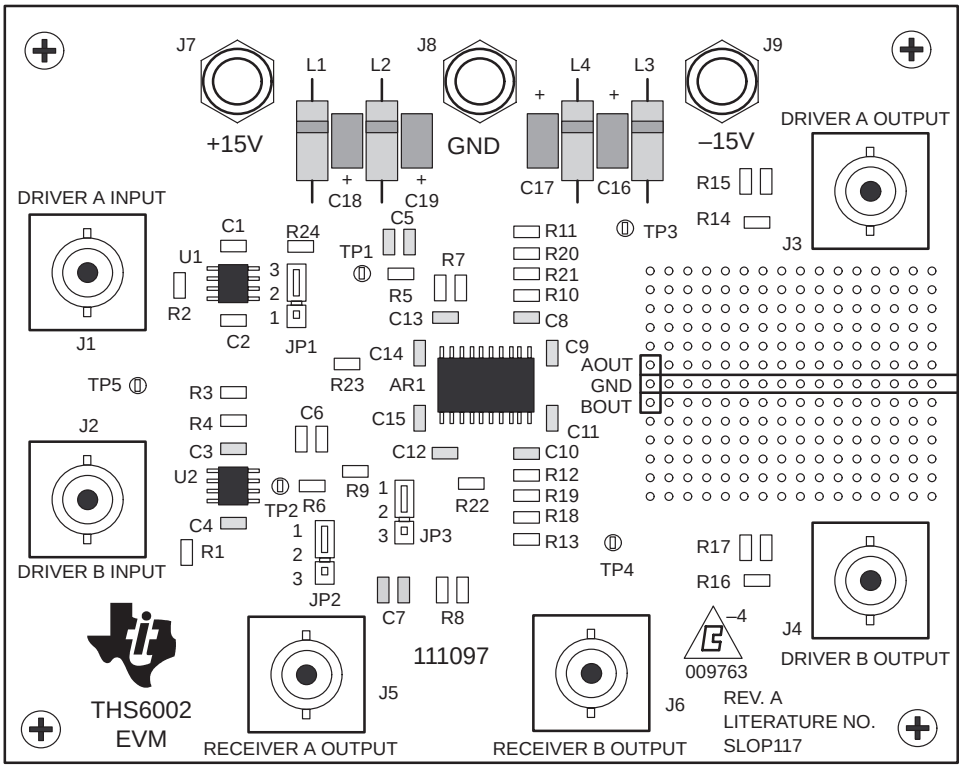
THS6002 Dual Differential Driver and Receiver EVM features include:

- A Complete ADSL Differential Line Driver and Receiver
- Multiple Input Configurations Set Via On-Board Jumpers
- Includes a Pair of THS4001 High-Speed Amplifiers as a Buffer and an Inverter
- Standard BNC Connectors Inputs and Outputs
- ±5-V to ±15-V Operation
- Nominal 50-Ω Impedance Inputs and Outputs
- Pad Area On Board For User Component Placement and Testing
- Good Example of PowerPAD Package and High-Speed Amplifier Design and Layout

1.2 Description

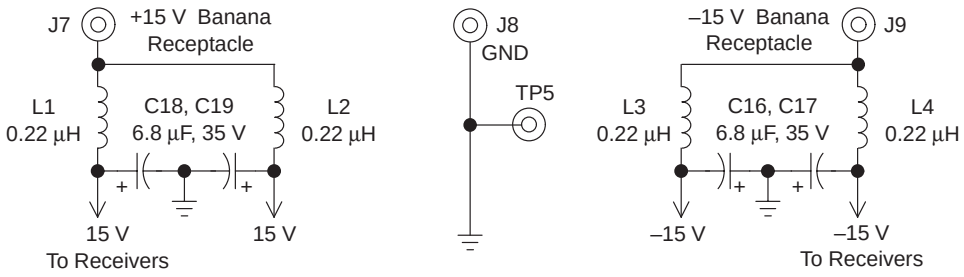
The TI THS6002 Dual Differential Line Driver and Receiver Evaluation Module (EVM) is a complete ADSL high-speed driver and receiver circuit. It consists of the TI THS6002 Dual Differential Line Drivers and Receivers IC, a pair of TI THS4001 High-Speed, Low-Power Operational Amplifier ICs, and a number of passive parts, all mounted on a multilayer circuit board (Figure 1–1). The EVM uses standard BNC connectors for inputs and outputs and also includes a pad area for user component connection and testing. It is completely assembled, fully tested, and ready to use — just connect it to power, a signal source, and a load (if desired).

Figure 1–1. THS6002 Evaluation Module



Input power is applied to the EVM through banana jacks J7, J8, and J9. Each power input is split into a separate power bus for the receivers, and a power bus for everything else on the module. An LC filter on each power bus isolates the receivers from the drivers and the EVM circuits from the external supply (Figure 1–2). The schematic for the EVM amplifiers appears in Figure 1–3.

Figure 1–2. THS6002 EVM Power Conditioning Schematic Diagram



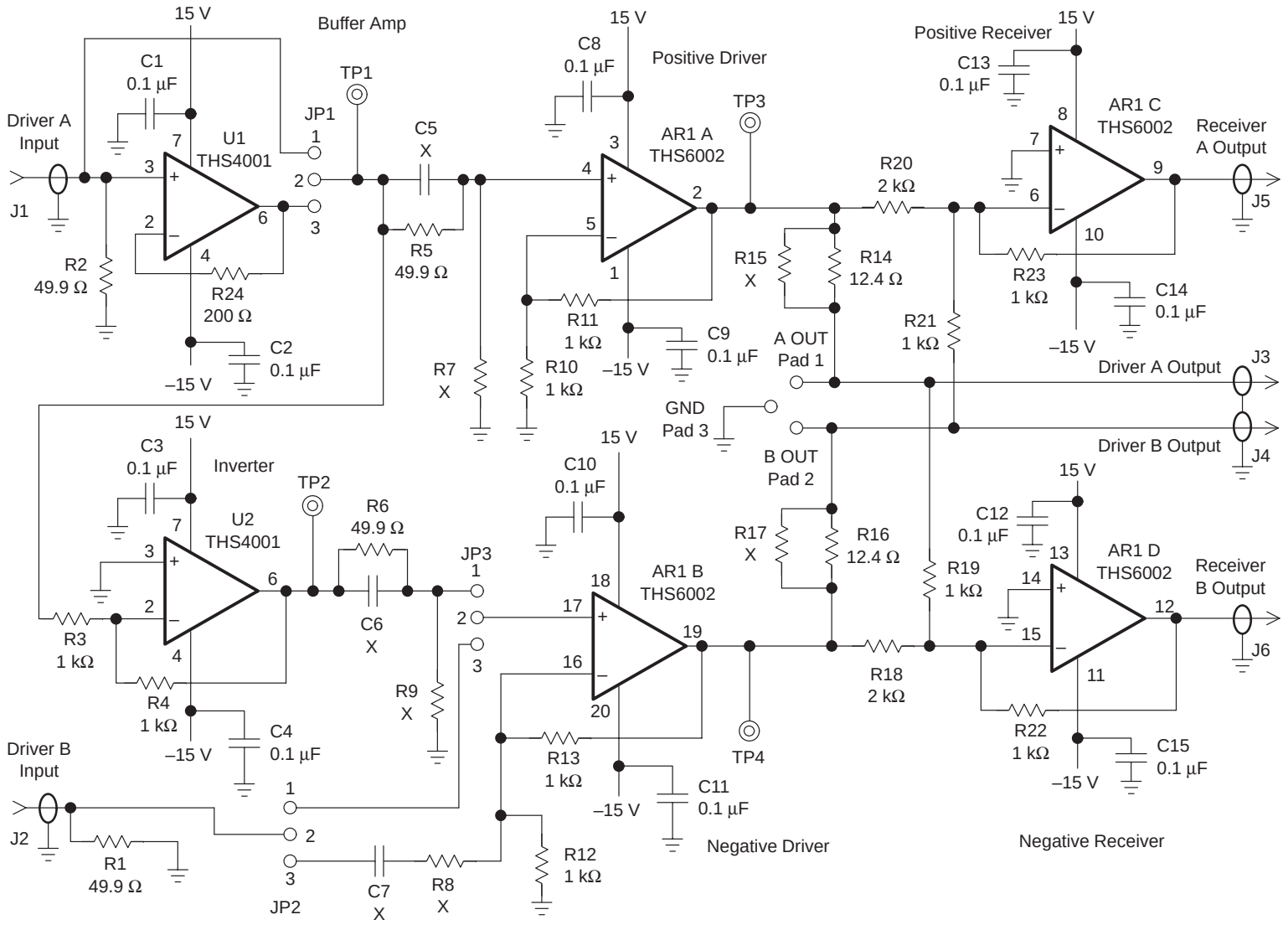


Figure 1–3. THS6002 EVM Schematic Diagram

The THS6002 EVM is equipped with a separate BNC connector for the driver A input and the driver B input. Each input is terminated with a 50-Ω resistor to provide correct line impedance matching (Figure 1–3). Note that using a source with a 50-Ω output impedance will create a voltage divider at the EVM inputs. Thus, accurate knowledge of the source output characteristics is required to determine proper input signal amplitudes.

Driver outputs are routed through ADSL-standard 12.5-Ω resistors to provide correct transmission line impedance matching when run through a 1:2 transformer with a 100-Ω termination. These resistors also allow the receivers to view a differential input signal from the transmission line.

The receivers do not have specific BNC inputs, but the EVM can be modified to individually evaluate the receivers. This requires the removal of R14, R16, R18, and R20. Because there are no output resistors connected to the receivers, care must be taken to avoid capacitive loading. This will decrease receiver phase margin, and peaking or oscillation may result.

All of the amplifiers on the EVM (THS6002 and THS4001) follow the classic operational amplifier gain equations:

$$\text{Inverting Gain} = \frac{-R_F}{R_G} \quad (1)$$

$$\text{Non-Inverting Gain} = 1 + \frac{R_F}{R_G} \quad (2)$$

The gain of the amplifiers can be easily changed to support different applications by changing resistor ratios. Any of the components on the EVM board can be replaced with different values. Also, component pads have been placed in convenient locations on the PCB (shown as components with the value X in the schematic) to allow numerous modifications to the basic EVM configuration. However, care must be taken because the surface mount solder pads on the board are somewhat fragile and will not survive a large number of soldering/desoldering operations.

The THS6002 IC is a current-feedback amplifier (CFB) and because of this, extra care must be taken to ensure that a feedback resistor is always included in the design. In addition, there must never be a capacitor directly in the feedback path between the noninverting input and the amplifier output. Disregarding this guideline will likely result in a part that oscillates. The THS4001 IC amplifiers used on the EVM, however, are classic voltage-feedback amplifiers (VFB) and have no restrictions on resistors or capacitors in the feedback path. But, to maximize bandwidth, high value resistors and capacitors should be used with discretion.

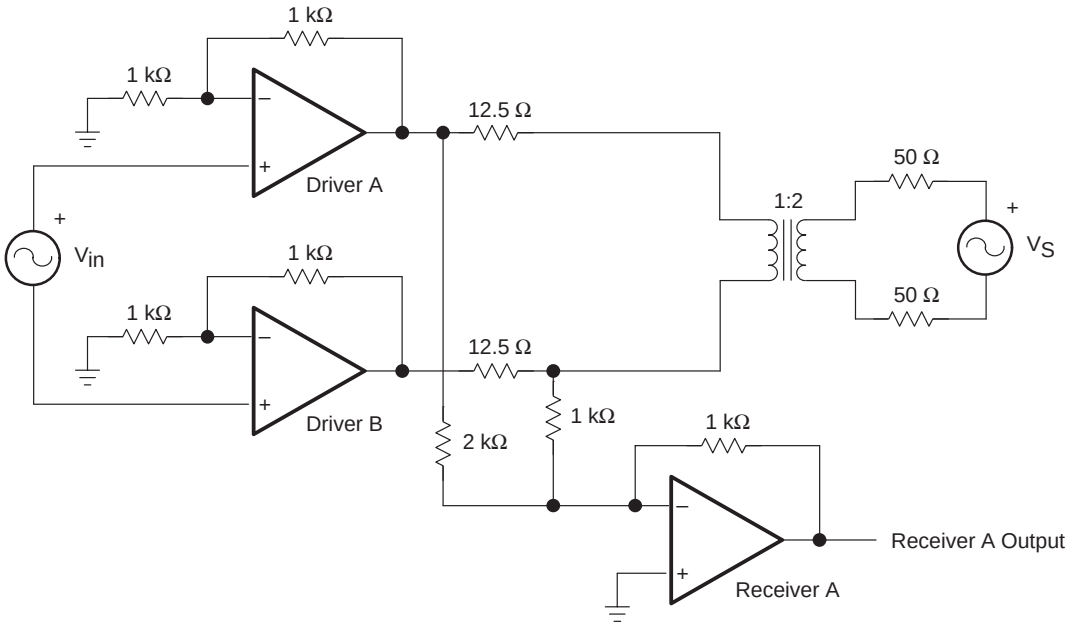
The THS6002 EVM is equipped with five testpoints (TP1 – TP5) to allow probing of the circuit at different points along the signal path. This should improve understanding of the signals involved in creating an ADSL transceiver and help solve any difficulties that might arise.

And finally, the EVM circuit board is a good example of proper board layout for high-speed amplifier and PowerPAD designs. It can be used as a guide for user application layouts.

1.3 Receiver Analysis

Receiver output prediction requires the understanding of all input signals to the device. Superposition is used here to help generate the output voltage equation for the receivers. Since the circuit is in a differential configuration (Figure 1–4), only receiver A is analyzed because the output of receiver B is simply the inverse of receiver A.

Figure 1–4. Receiver Analysis Schematic



The first source to receiver A is the output of driver A ($V_{DRV–A}$). This follows the basic inverting equation (Equation 1).

$$\text{Receiver-A Output (1)} = V_{\text{DRV-A}} \times \frac{-1\ \text{k}\Omega}{2\ \text{k}\Omega} \tag{3}$$

The second source is the output of driver B ($V_{DRV–B}$). When the 50-Ω termination resistors are transferred to the primary side, each driver *sees* 12.5 Ω of impedance in addition to the existing 12.5-Ω resistors. Therefore, only one-half the voltage output of driver B reaches receiver A because of the voltage division among the 12.5-Ω resistor and the 12.5-Ω transformer impedance.

$$\text{Receiver-A Output (2)} = \frac{V_{\text{DRV-B}}}{2} \times \frac{-1\ \text{k}\Omega}{1\ \text{k}\Omega} \tag{4}$$

The third source is the signal from the transmission line (V_S). The voltage at the transformer is one-half the source voltage (V_S) due to the impedance matching. When referred back to the primary side, the signal voltage is again one-half the transformer voltage as a result of the 1:2 transformer ratio. It is also inverted since the signal comes from the low side of the transformer. And

finally, because of the impedance division shown above, the source signal is once again divided in half for a total of 1/8 V_S.

$$\text{Receiver-A Output (3)} = \frac{-V_S}{8} \times \frac{-1\ k\Omega}{1\ k\Omega} \qquad (5)$$

Summing all three output equations together:

$$\text{Receiver-A Voltage Output} = -1/2\ V_{DRV\text{-}A} - 1/2\ V_{DRV\text{-}B} + 1/8\ V_S \qquad (6)$$

Because the output of driver B is the inverse of driver A, the first two parts of Equation 6 cancel out, leaving:

$$\text{Receiver-A Voltage Output} = 1/8\ V_S \qquad (7)$$

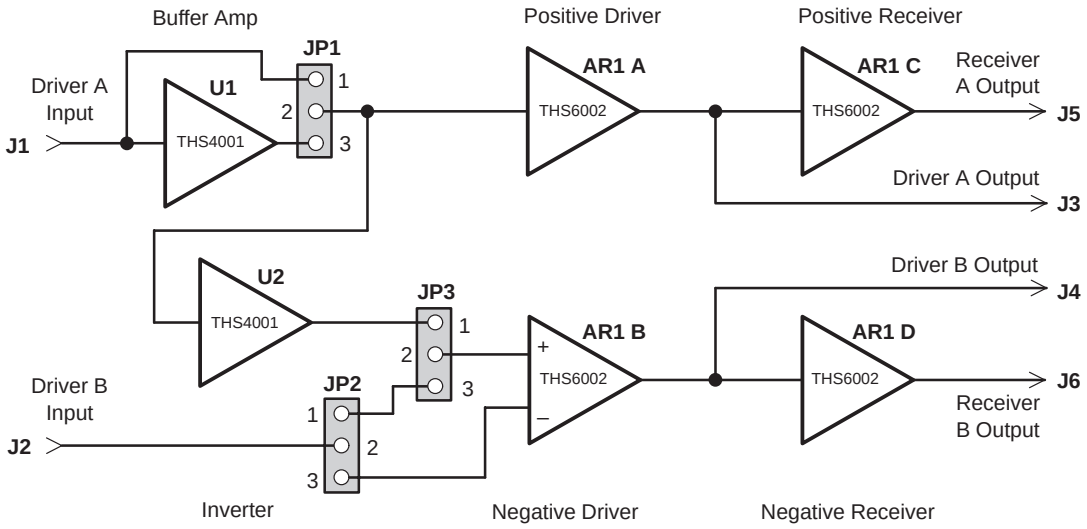
and

$$\text{Receiver-B Voltage Output} = -1/8\ V_S$$

1.4 Input Configuration

The THS6002 EVM inputs can be configured in several different ways to provide a wide variety of circuits to support different applications (Figure 1–5). Each of the three jumpers on the EVM is a three-pin header that is used as a SPDT switch by placing a shunt across two pins to select either of two possible signal routes.

Figure 1–5. THS6002 Evaluation Module Block Diagram



- ❑ Jumper JP1:
  - ■ 1–2 — bypasses the THS4001 buffer amplifier (U1) when using driver A input connector (J1)
  - ■ 2–3 — routes the signal through the THS4001 buffer amplifier (U1) when using driver A input connector (J1)
- ❑ Jumper JP2:
  - ■ 1–2 — connects the driver B input connector (J2) to the noninverting input of driver B when jumper J3 is set appropriately
  - ■ 2–3 — connects the driver B input connector (J2) to the inverting input of driver B when jumper JP3 is set appropriately
- ❑ Jumper JP3:
  - ■ 1–2 — connects the noninverting input of driver B (AR1 B) to the THS4001 inverting amplifier (U2) output
  - ■ 2–3 — connects the noninverting input of driver B (AR1 B) to the input connector (J2) when jumper JP2 is set appropriately

For example, to use a single-ended input, jumper JP3 should be set to 1–2 and the input signal applied to input connector J1. The output of the THS6002 drivers is a differential signal due to the inverter (U2) and JP3 being set to 1–2. For a differential source, JP3 should be set to 2–3, JP2 should be set to 1–2 and the differential input signal applied between input connectors J1 and J2.

Note that if JP2 is in the 2–3 position, components C7, R8, and R9 must be installed, JP3 must be set to 1–2, and R6 must be removed for proper operation.

1.5 THS6002 EVM Specifications

Supply voltage range, $\pm V_{CC}$ . . . . . ±5 V to ±15 V
Supply current, I_{CC} . . . . . 48 mA
Input voltage, V_I . . . . . ±VCC, max
Output drive, THS6002 Drivers, I_O . . . . . 500 mA, typ
Output drive, THS6002 Receivers, I_O . . . . . 85 mA, typ
Continuous total power dissipation at TA = 25°C (THS6002), ... 5.8 W, max

For complete THS6002 amplifier IC specifications and parameter measurement information, and additional application information, see the THS6002 data sheet, TI Literature Number SLOS202.

1.6 Using The THS6002 EVM

The THS6002 EVM operates from a split power supply with voltages ranging from ±5 V to ±15 V. The use of a single supply for this EVM is not recommended. As shipped, the output of driver A (at TP3) is equal to a noninverting gain of 2 when using the single-ended input mode. The output of driver B (at TP4) is equal to an inverting gain of 2 under the same conditions. An oscilloscope is typically used to view and analyze the EVM output signals.

1) Ensure that all power supplies are set to ***OFF*** before making power supply connections to the THS6002 EVM.

2) Select the operating voltage for the EVM and connect appropriate split power supplies to the banana jacks on the module marked ***+15V*** (J7) and ***–15V*** (J9)***.***

3) Connect the power supply ground to the module banana jack marked ***GND*** (J8).

4) Connect an oscilloscope probe to TP3. This is the driver A amplifier output. Connecting directly to the **DRIVER A OUTPUT** BNC connector (J3) with a 50-Ω nominal impedance cable and probe is not recommended. The source impedance of driver A is only 12.5 Ω and such a connection will cause reflections to occur at high frequencies and is not a true measurement of the amplifier performance.

5) Set jumper J1 to the 2–3 position.

6) Set jumper J2 to the 1–2 position.

7) Set jumper J3 to the 1–2 position.

8) Set the power supply to ***ON***

9) Connect a signal input to the **DRIVER A INPUT** BNC (J1).

Note that each input connector on this EVM is terminated with a 50-Ω resistor to ground. With a 50-Ω source impedance, the voltage seen by the THS6002 amplifier IC on the EVM will be ½ the source signal voltage applied to the EVM input connector.

10) Verify the output signal on the oscilloscope.

Without an effective 25-Ω impedance between the outputs of the drivers, the receiver outputs will not behave as previous equations predict. For a quick check to verify that the receivers are indeed working properly, solder a 25-Ω resistor from the output of driver A to the output of driver B. Ensure that the power rating of the resistor is sufficient to handle the 500 mA of current that the drivers are capable of producing.

1.7 THS6002 EVM Performance

Figure 1–6 shows the typical frequency response of the THS6002 EVM drivers when properly loaded. This data was collected using a single-ended input with JP1 set to 1–2 and with a 25-Ω load connected between the driver outputs, as shown in the test circuit of Figure 1–7.

Typical unity gain bandwidth with a ±15 V power supply is 105 MHz for driver B and 180 MHz for driver A. With a ±5 V power supply, typical unity gain bandwidth is 100 MHz for driver B and 130 MHz for driver A. The difference between the output signals of driver A and driver B is primarily due to the high-frequency characteristics of the inverting amplifier (U2). Component values can be changed to cause the two responses to track more closely, but since ADSL signals are limited to 2 MHz and below, the high-frequency imbalance can usually be ignored.

Figure 1–6. THS6002 EVM Driver Frequency Response With a 25-Ω Load

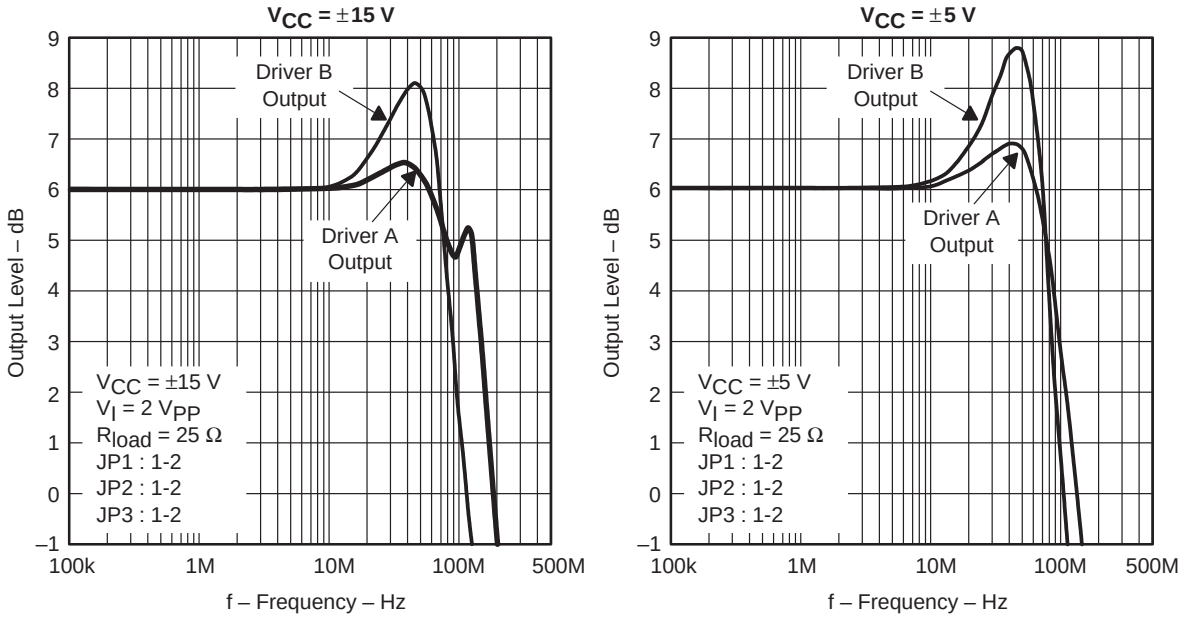


Figure 1–7. THS6002 EVM Driver Frequency Response Test Circuit

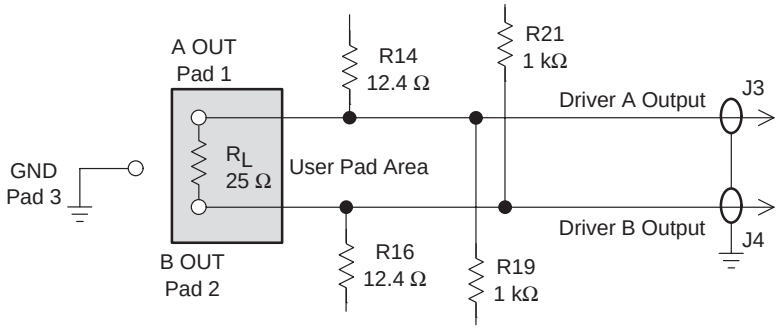


Figure 1–8 shows the typical frequency response of the THS6002 EVM receivers. This data was collected with the receiver loaded with an external 150-Ω resistor connected to the receiver output BNC as shown in the test circuit of Figure 1–9. Typical –3 dB bandwidth is 70 MHz with either a ±5 V or a ±15 V power supply.

Figure 1–8. THS6002 EVM Receiver Frequency Response

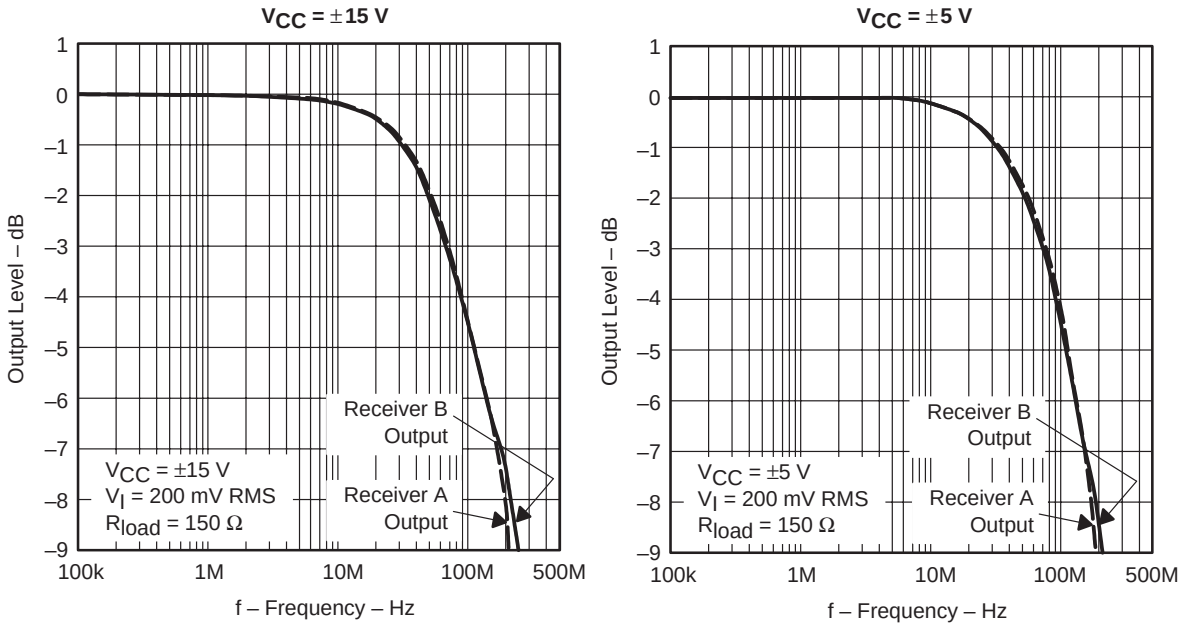


Figure 1–9. THS6002 EVM Receiver Frequency Response Test Circuit

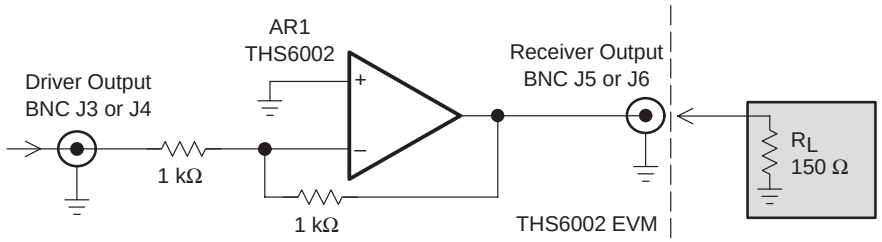


Figure 1–10 shows the typical receiver rejection of the driver signals. The driver outputs are connected together through a 25-Ω resistor mounted on the PCB user pads and the receivers are loaded with external 150-Ω resistors connected to BNC connectors J5 and J6 as shown in Figure 1–11. The input signal level is 200 mV rms.

The outputs do not exactly cancel because of resistor mismatches and also because driver B is driven through an inverting stage. Rejection at 1 MHz is typically – 30 dB for both ±15 V and ±5 V power supplies. There are several techniques that will increase the rejection further, but they are beyond the scope of this simple EVM.

Figure 1–10. THS6002 EVM Receiver Rejection

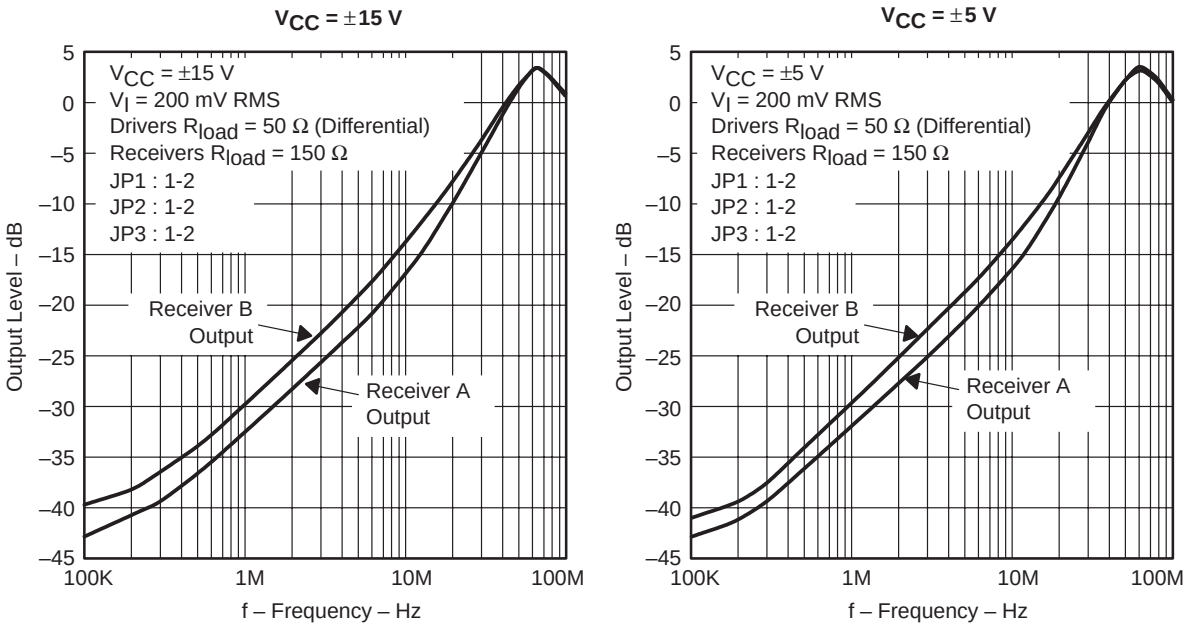
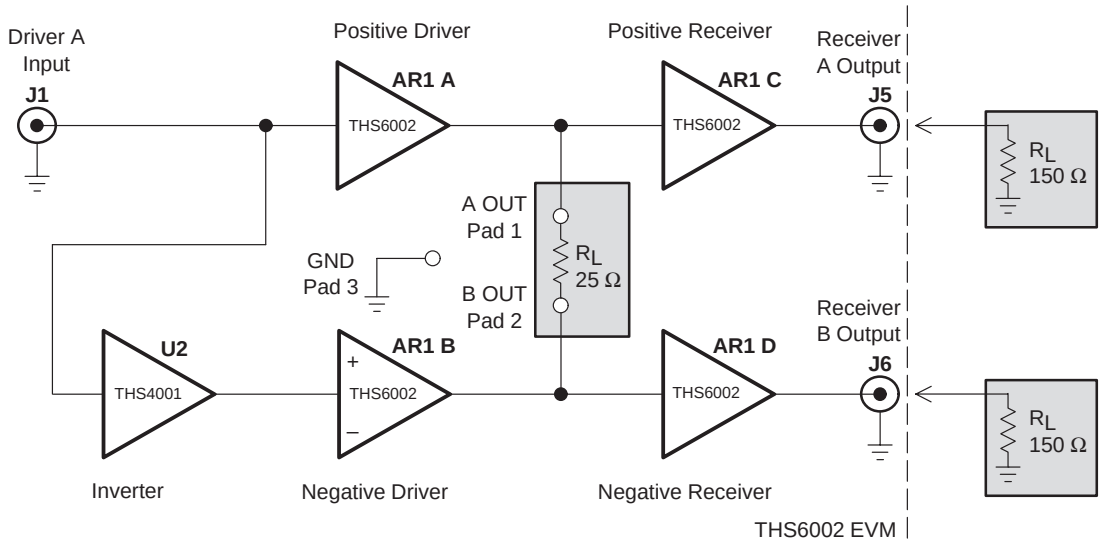


Figure 1–11. THS6002 EVM Receiver Rejection Test Circuit



1.8 General High-Speed Amplifier Design Considerations

The THS6002 EVM layout has been designed and optimized for use with high-speed signals and can be used as an example when designing THS6002 applications. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Disregard of these basic design considerations could result in less than optimum performance of the THS6002 dual differential line drivers and receivers IC.

Surface mount components were selected because of the extremely low lead inductance associated with this technology. Also, because surface mount components are physically small, the layout can be very compact. This helps minimize both stray inductance and capacitance.

Tantalum power supply bypass capacitors (C16 through C19) at the power input pads help supply currents for rapid, large signal changes at the amplifier output. The 0.1 μF power supply bypass capacitors (C1 through C4 and C8 through C15) were placed as close as possible to the IC power input pins in order to keep the PCB trace inductance to a minimum. This improves high-frequency bypassing and reduces harmonic distortion.

A proper ground plane should always be used with high-speed circuit design. This provides low-inductive ground connections for return current paths. Special attention is needed for the inverting input pins. Stray capacitance at these pins can seriously degrade the performance of the amplifiers. In addition, ground plane coupling into these pins can cause noise to appear at the outputs of the amplifiers. This is especially important for the inverting pin while the amplifier is operating in the noninverting mode. Because the voltage at this pin swings directly with the noninverting input voltage, any stray capacitance would allow currents to flow into the ground plane, causing possible gain error and/or oscillation. Capacitance variations at the amplifier IC input pin of less than 1 pF can significantly affect the response of the amplifier.

In general, it is always best to keep signal lines as short and as straight as possible. Sharp 90° corners should generally be avoided — round corners or a series of 45° bends should be used, instead. Stripline techniques should also be incorporated when signal lines are greater than 3 inches in length. These traces should be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Such signal lines should also be properly terminated with an appropriate resistor.

Finally, proper termination of all inputs and outputs should be incorporated into the layout. Unterminated lines, such as coaxial cable, can appear to be a reactive load to the amplifier IC. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears to be purely resistive, and reflections are absorbed at each end of the line. Another advantage of using an output termination resistor is that capacitive loads are isolated from the amplifier output. This isolation helps minimize the reduction in amplifier phase-margin and improves the amplifier stability for improved performance such as reduced peaking and settling times.

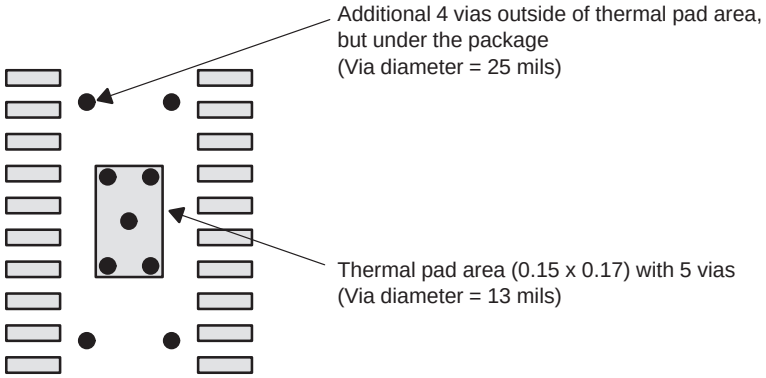
1.9 General PowerPAD Design Considerations

The THS6002 IC is mounted in a special package incorporating a thermal pad that transfers heat from the IC die directly to the PCB. The PowerPAD package is constructed using a downset leadframe. The die is mounted on the leadframe but is electrically isolated from it. The bottom surface of the lead frame is exposed as a metal thermal pad on the underside of the package and makes physical contact with the PCB. Because this thermal pad is in direct physical contact with both the die and the PCB, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad mounting point on the PCB.

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach as used on the THS6002 EVM, which is built on a multilayer PCB with an internal ground plane.

1) Prepare the PCB with a top side etch pattern as shown in Figure 1–12. There should be etch for the leads as well as etch for the thermal pad.

Figure 1–12. PowerPAD PCB Etch and Via Pattern



2) Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.

3) Place four more holes under the package, but outside the thermal pad area. These holes are 25 mils in diameter. They may be larger because they are not in the area to be soldered so that wicking is not a problem.

4) Connect all nine holes, the five within the thermal pad area and the four outside the pad area, to the internal ground plane.

5) When connecting these holes to the ground plane, do **not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6002 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.

6) The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its five holes. The four larger holes outside the thermal pad area, but still under the package, should be covered with solder mask.
7) Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
8) With these preparatory steps in place, the THS6002 is simply placed in position and run through the solder reflow operation as any standard surface mount component. This results in a part that is properly installed.

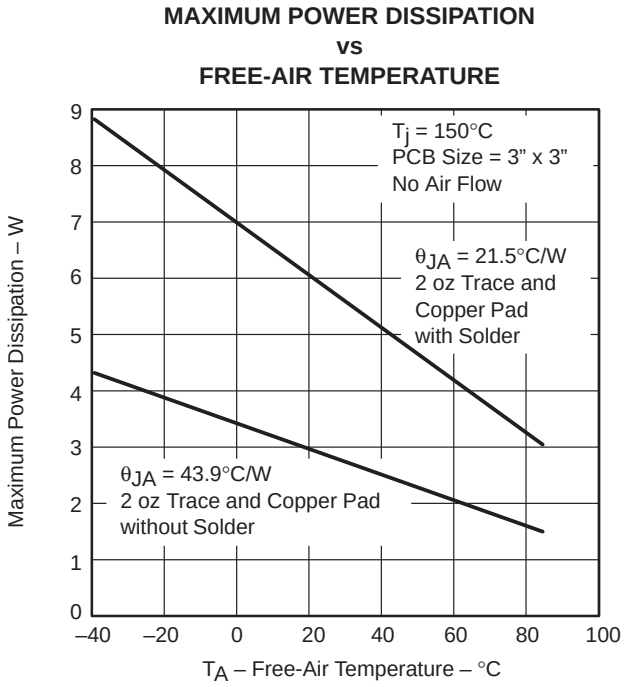
The actual thermal performance achieved with the THS6002 in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches $\times$ 3 inches, then the expected thermal coefficient, θ_{JA}, is about 21.5°C/W. For a given θ_{JA}, the maximum power dissipation is shown in Figure 1–13 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6002 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = Thermal coefficient from die junction to ambient air (°C/W)

Figure 1–13. Maximum Power Dissipation vs. Free-Air Temperature



Even though the THS6002 EVM PCB is larger than the one in the example above, the results should correlate very well because the traces and the vias of the EVM PCB interrupt the thermal continuity of the ground plane. The THS6002 EVM is a good example of proper thermal management when using PowerPAD-mounted devices.

Correct PCB layout and manufacturing techniques are critical for achieving adequate transfer of heat away from the PowerPAD IC package. More details on proper board layout can be found in the *THS6002 DUAL DIFFERENTIAL LINE DRIVERS AND RECEIVERS* data sheet (SLOS202). For more general information on the PowerPAD package and its thermal characteristics, see the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package* (SLMA002).

Chapter 2

Reference

This chapter includes a parts list and PCB layout illustrations for the THS6002 EVM.

Topic **Page**

2.1 THS6002 Dual Differential Line Drivers and Receivers EVM Parts List

Table 2–1. THS6002 EVM Parts List

Reference	Description	Size	Quantity	Manufacturer/Distributor Part Number
C16,C17, C18,C19	CAPACITOR, 6.8 μF, CERAMIC, 20%, TANTALUM, SM		4	(SPRAGUE) 293D685X9035D2T
C1–C4, C8–C15	CAPACITOR, 1 μF, CERAMIC, 10%, SM	1206	12	(SPRAGUE) 11C1210E104M5NT
L1,L2,L3, L4	INDUCTOR, 0.22 μH AXIAL, THRU HOLE		4	(DELEVAN) DN41221/ (DIGI-KEY) DN41221-ND
J1,J2,J3, J4,J5,J6	CONNECTOR, BNC 50 OHM VERTICAL PC MOUNT, THRU HOLE		6	(AMP) 227699-1, -2/ (ALLIED) 512-2130, 512-2200
J7,J8,J9	JACK, BANANA RECEPTACLE, FOR 0.025″ DIA. HOLE		3	(NEWARK) 35F865
JP1,JP2, JP3	HEADER, 3 PIN, 0.1″ CTRS., 0.025″ SQ. PINS		3	
P1,P2,P3	SHORTING JUMPERS, 0.1″ CTRS, FOR 0.025″ SQ. PINS		3	
R1,R2,R5, R6	RESISTOR, 49.9 OHM, 1/8W, 1% SM	1206	4	
R3,R4, R10–R13, R19,R21–R23	RESISTOR, 1 K OHM, 1/8W, 5% SM	1206	10	
R14,R16	RESISTOR, 12.4 OHM, 1/8W, 1% SM	1206	2	
R18,R20	RESISTOR, 2 K OHM, 1/4W, 5% SM	1206	2	
AR1	IC, THS6002CDWP		1	(TI) THS6002CDWP
U1,U2	IC, OP AMP, THS4001CD	SOIC-8	2	(TI) THS4001CD
TP1,TP2, TP3,TP4	TEST POINT, (RED)		4	(FARNELL) 240-345
TP5	TEST POINT, (BLACK)		1	(FARNELL) 240-333
R7,R8,R9, R15,R17	RESISTOR, X OHMS, SM†	1206	5	
C5,C6,C7	CAPACITOR, X μF, 10% CERAMIC†		3	
PCB1	PCB, THS6002 EVM SLOP117		1	

† The values of these components are to be determined by the user in accordance with the application requirements.

2.2 THS6002 EVM Board Layouts

Board layout examples of the THS6002 EVM PCB are shown in the following illustrations. They are not to scale and appear here only as a reference.

Figure 2–1. THS6002 EVM Component Placement Silkscreen and Solder Pads

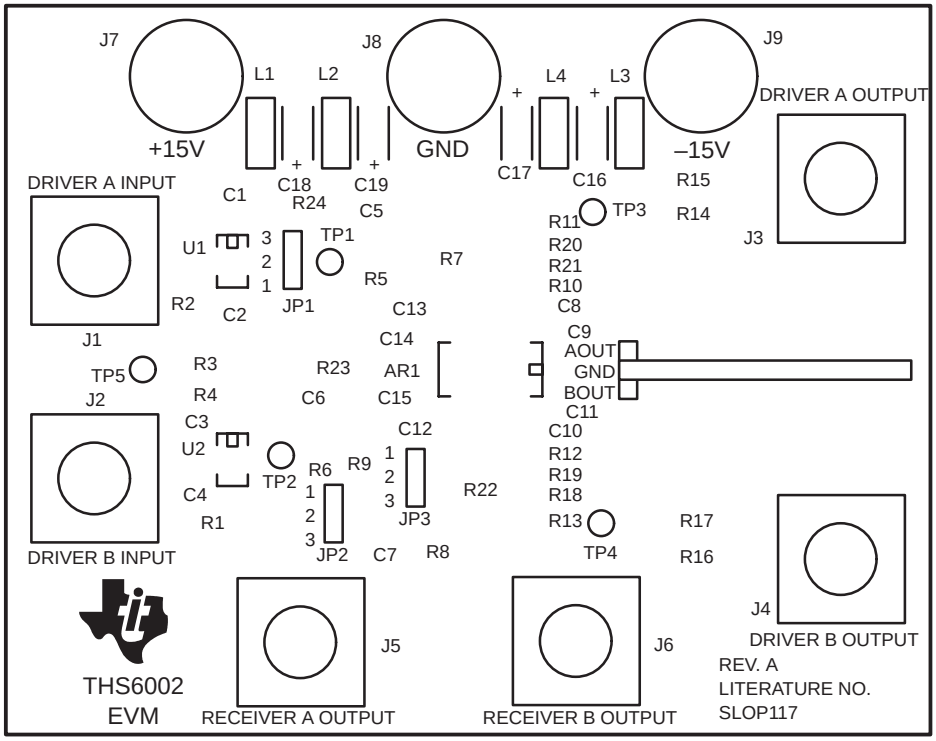


Figure 2–2. THS6002 EVM PC Board: Layer 1 — Top Side Layout

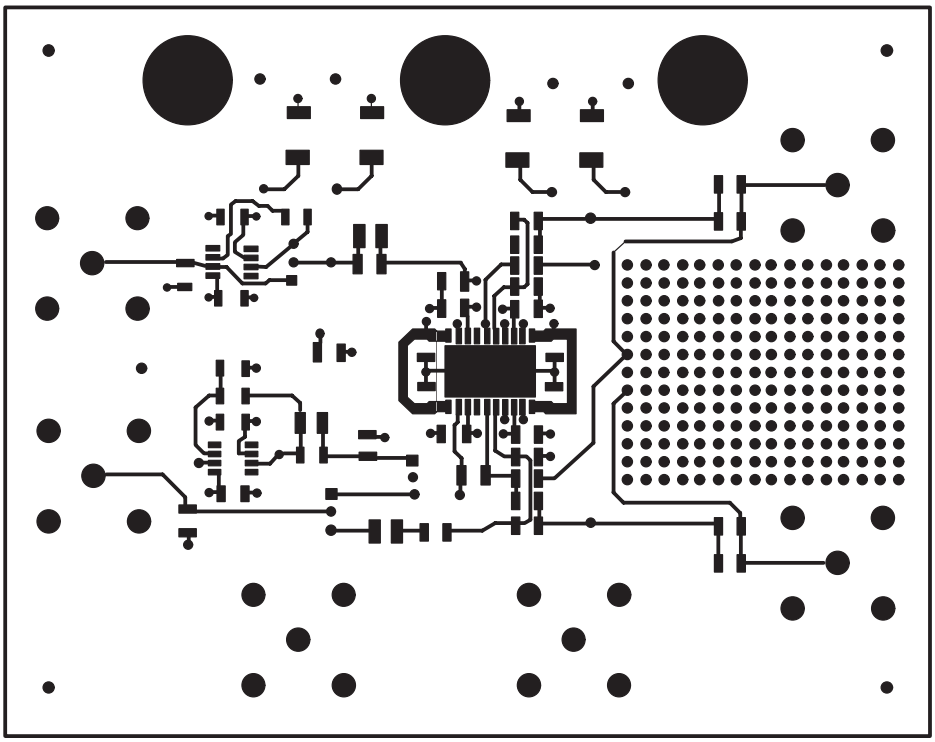


Figure 2–3. THS6002 EVM PC Board: Layer 2 — Ground Plane Layout

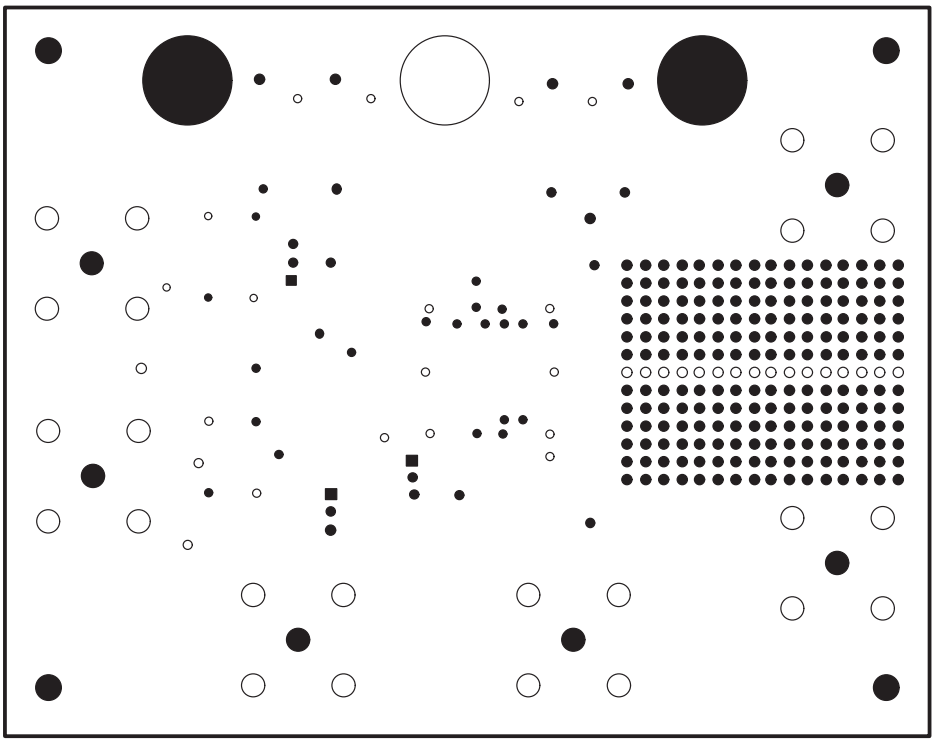


Figure 2–4. THS6002 EVM PC Board: Layer 3 — Signal Layout

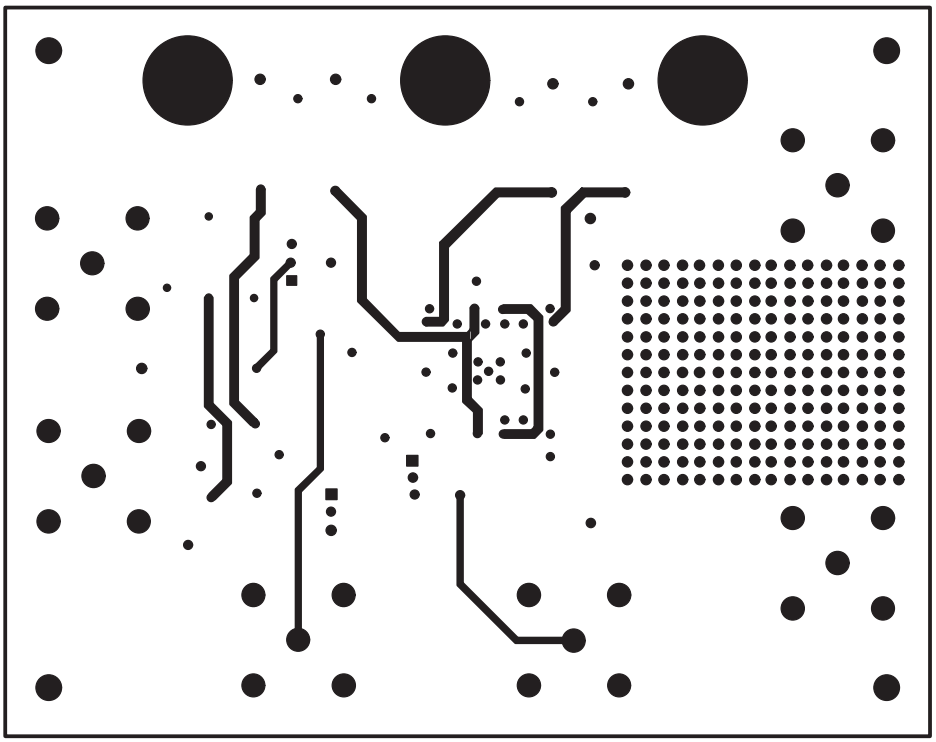


Figure 2–5. THS6002 EVM PC Board: Layer 4 — Back Side Layout

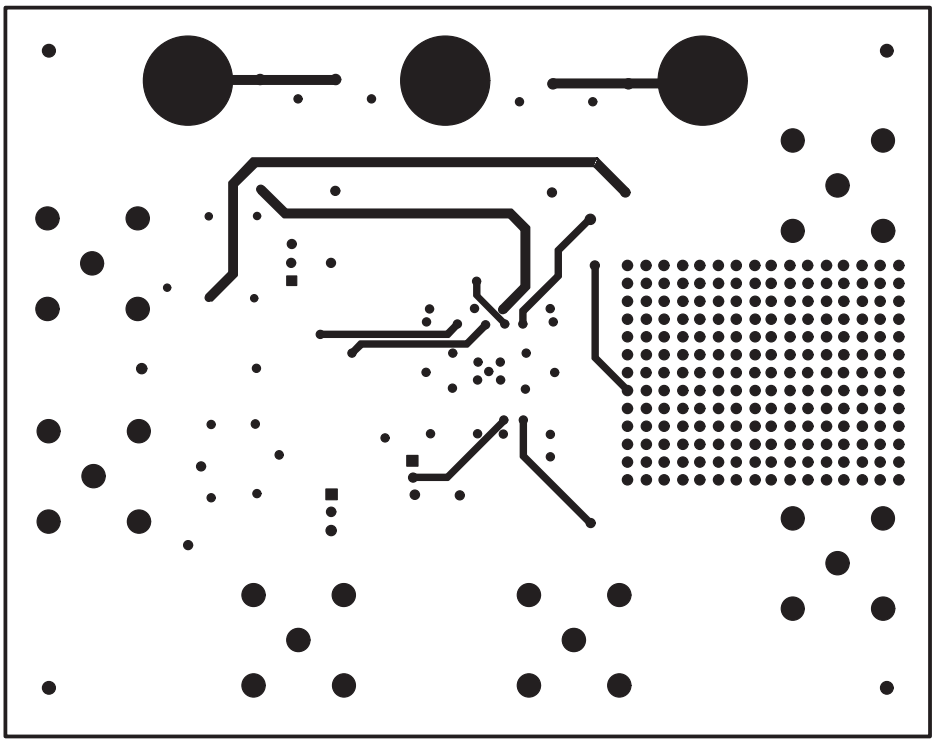


Figure 2–6. THS6002 EVM PC Board: Solder Mask — Top Side

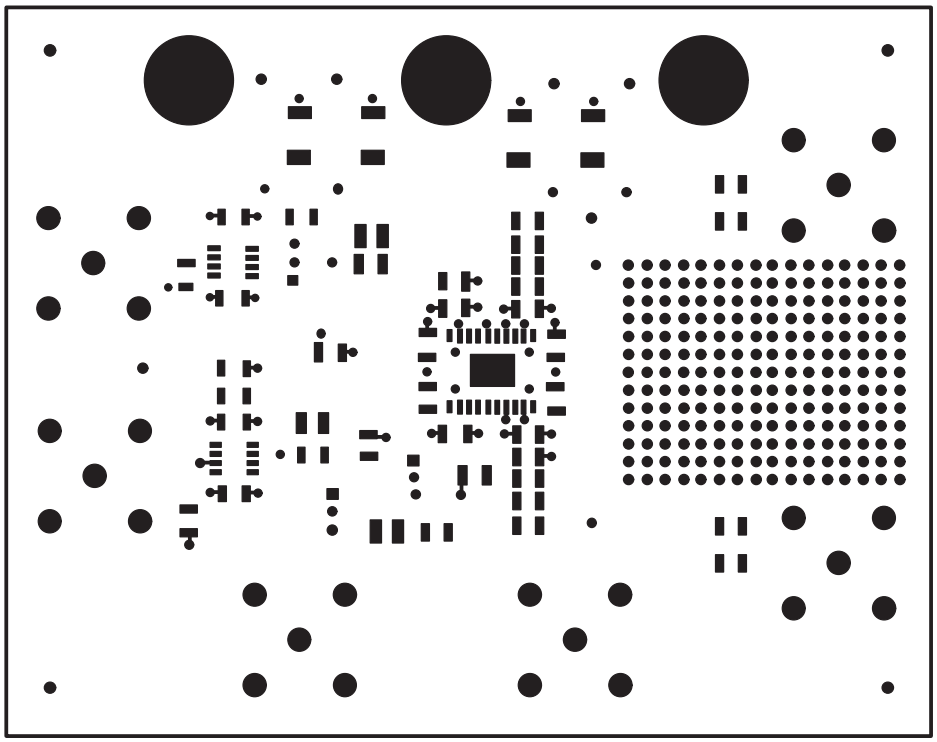


Figure 2–7. THS6002 EVM PC Board: Solder Mask — Back Side